REMARKS/ARGUMENTS

In this non-final Action, the Examiner objected to claims 1-2, and 5 for informalities in the claim wording. In response, applicant has amended claims 1-5 to cure the informalities. The informalities resulted from claim words that were deleted by the amendment dated November 2, 2006, reappearing in the claims. The current amendment restores the claims to what they should have been following the amendment of November 2, 2006. Applicant therefore requests that the objection to the claims as amended be withdrawn.

The Examiner indicated that claim 4 would be allowable if placed in independent form. Applicant has done so, presenting the independent form of claim 4 as new claim 6. The subject matter recited in claim 4 is a detailed recitation of the subject matter of the last two sub-elements of claim 3 from which claim 4 depended, and therefore the two sub-elements of claim 3 have been omitted from claim 6 to avoid duplication. Applicant therefore requests that claim 6 be allowed.

The Examiner rejected claims 1-3 and 5 under 35 U.S.C. §103 over U.S. patent no. 7,072,880 (Beesley) in view of U.S. patent no. 5,630,130 (Perotto et al.). In response, applicant has amended these claims to define with particularity the constitution of a merged or augmented finite-state machine. As amended, the claims recite that a merged machine represents a plurality of single-counter finite-state machines each representing a different one of a plurality of counters and wherein at least one state of the merged finite-state machine each corresponds to a multiplicity of states each of a different one of said single-counter finite-state machines. Support for this amendment is found at, e.g., page 3, line 17; page 7, line 23; and page 8, lines 6-11.

In contrast, Beesley discloses a transducer/acceptor/network that comprises a plurality of state machines that are strung together serially (see, e.g., Fig. 11). The transducer/acceptor/network corresponds to strings/words, while each state machine corresponds to a domain of sub-

strings/formants. Since the transducer/acceptor/network is a concatenation of finite-state machines, the transducer/acceptor/network does not have at least one state each corresponding to a multiplicity of states of a different one of the finite-state machines. Consequently, the transducer/acceptor/network is also not augmented with state value lists – the concept of a state value list is not applicable to the structure of a transducer/acceptor/network of Beesley.

The Examiner did concede that "Beesley does not explicitly teach using multi-counters," and cited Perotto et al. for this teaching. But the combination of Beesley and Perotto et al. likewise fails to teach applicant's claimed invention.

Perotto et al. disclose a multitasking controller that has a separate program counter, a separate accumulator, and a separate index register, for each one of a plurality of tasks. Thus, there is a bank of a plurality of individual program counters, another bank of a plurality of individual accumulators, and another bank of a plurality of individual index registers. A program counter points to a memory location containing the next instruction that is to be executed of its corresponding task (column 4, lines 4-6). An accumulator holds data associated with its corresponding task for use by the arithmetic and logic unit (column 5, lines 31-34). An index register stores an address employed by its corresponding task as an offset value for indexed addressing (column 5, lines 1-2 and 38-40).

Perotto et al. bear no relation either to Beesley or to applicant's claimed invention. Perotto et al. are concerned with efficient operation of a multitasking controller, and not with the substring-number mapping of Beesley or with multi-counter evaluation like applicant. Nor do Perotto et al. disclose a multi-counter, as is made evident by the above discussion of the disclosure of Perotto et al.

Nevertheless, even if one assumes for purposes of argument that Perotto et al. do disclose a multi-counter, Perotto et al. still fail to cure the fundamental failure of Beesley to disclose, teach, or suggest the claimed

invention. Specifically, the combined teachings of Beesley and Perotto et al. fail to disclose, teach, or suggest a merged or augmented finite-state machine as defined in the amended claims or at least a state-value list and augmentation therewith of the merged or augmented finite-state machine, as is required in one form or another by the recitation of all applicant's amended claims.

For the reasons given above, applicant asserts that the combined teachings of Beesley and Perotto et al. do not render applicant's claims unpatentable. Applicant therefore requests that the Section 103(a) rejection of his claims be withdrawn.

The Examiner's objections and rejection having been properly responded to and overcome, applicant suggests that the application is now in condition for allowance. Applicant therefore requests that the application be reconsidered and thereafter be passed to issue.

Applicant considers the foregoing to be dispositive of all issues in the application. But if the Examiner should deem that a telephone interview would advance the prosecution, he is invited to call applicant's attorney at the telephone number listed below.

Respectfully submitted,

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